

Prior art EEPROM devices only allow the voltage supplied to the control gate  $V_{CG}$  to assume one of two voltages, namely  $V_{CC}$  or the higher programming voltage of about 12V.

In another aspect of the present invention, the voltage supplied to the control gate  $V_{CG}$  is allowed to be independently and continuously variable over a wide range of voltages. This is provided by  $V_{PG}$  from the controller 1140. In particular  $V_{CG}$  in a line 1083 is fed from  $V_{PG}$  which is in turn supplied by the controller from a line 1901. Figure 27 shows  $V_{PG}$  to assume various voltages under different functions of the EEPROM.

The variability of  $V_{CG}$  is particularly advantageous in program and erase margining schemes. In program margining, the read during program verify is done with  $V_{CG}$  at a slightly higher voltage than the standard  $V_{CC}$ . This helps to place the programmed threshold well into the state by programming past the breakpoint threshold level with a slight margin. In erase verify, the cell is verified with a somewhat reduced  $V_{CG}$  to put the cell well into the "erased" state. Furthermore, margining can be used to offset the charge retention problem described earlier (Figure 16B).

As mentioned before, prior art EEPROMs typically employ  $V_{CC}$  to feed  $V_{CG}$  during program or erase verify. In order to do margining,  $V_{CC}$  itself needs to be ramped up or reduced. This practice produces inaccurate results in the reading circuits since they are also driven by  $V_{CC}$ .

In the present invention, the variability of  $V_{CG}$  independent of voltages supplied to the reading circuit produce more accurate and reliable results.

Furthermore, the wide range of  $V_{CG}$  is useful during testing and diagnostic of the EEPROM. It allows the full range of the programmed cell's threshold to be measured easily by continuing to increase  $V_{CG}$  (up to the maximum limited by the device's junction breakdown) --

#### IN THE DRAWINGS:

Add the accompanying sheets 6-22 of drawings, in informal form, which contain additional Figures 9-27.

#### IN THE CLAIMS:

Please cancel the original parent application claims 1-62, without prejudice, and substitute the following new claims therefore:

Sub B3 -63. A semiconductor disk device comprising:

a non-volatile, electronically programmable and erasable flash memory including a plurality of blocks, each block having a plurality of sectors and being a unit of erasure for the flash memory;